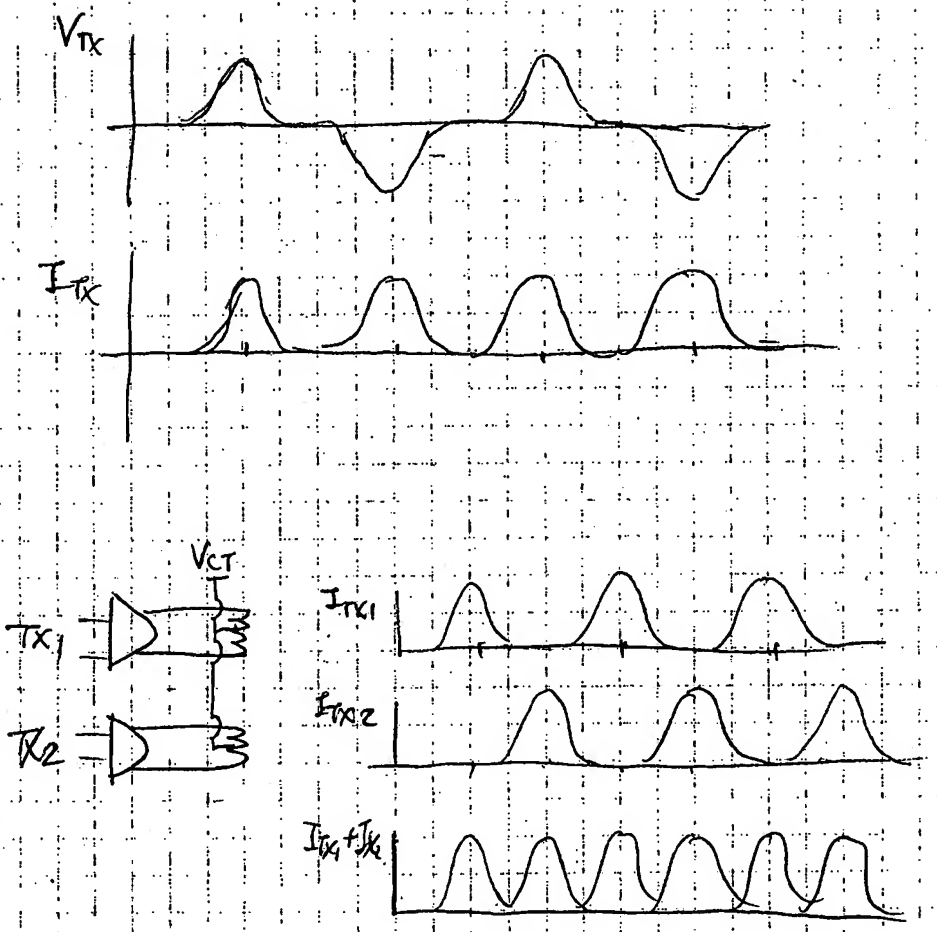
EXHIBIT B

[redacted]

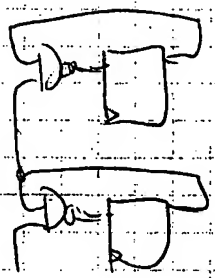
EMI

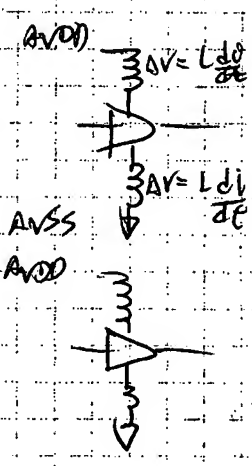


Mixing clock phase

- ✓ local — pair to pair — adjacent pairs
- ✓ global — port to port — Multi ports
  Adjacent phy.

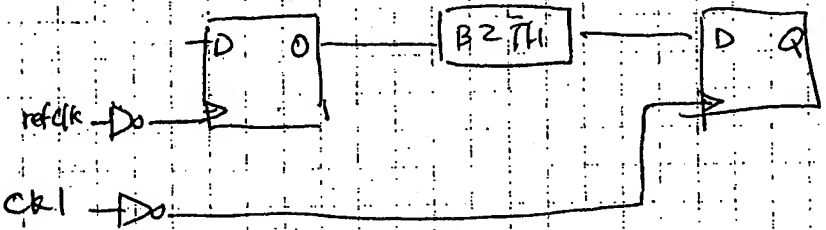
- reduce EMI
- reduce requirement for Common-mode Choke

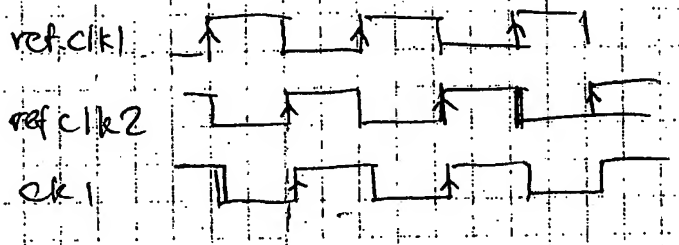




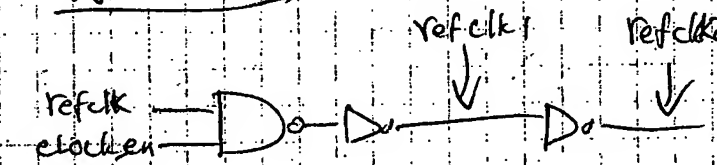
Improvement → - Reduce Power supply bounce
- Reduce EMI (Clock switch a different time).

Decoder



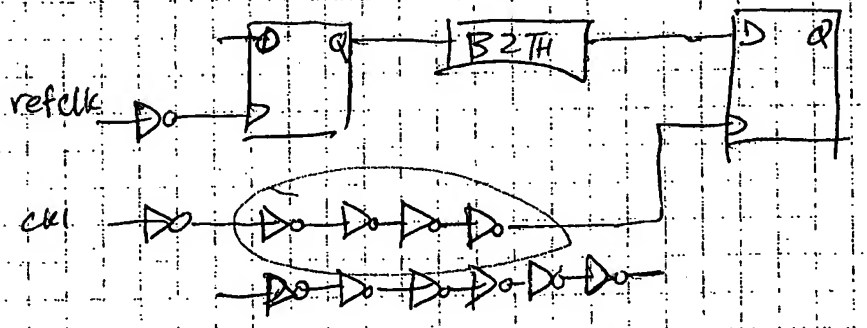


- refclk 2 (inverted from refclk1) is the input to DLL giving 180° Shift.



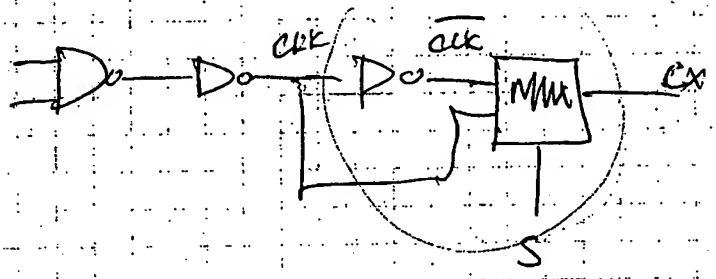
Changes

① Change decoder to have clock delay

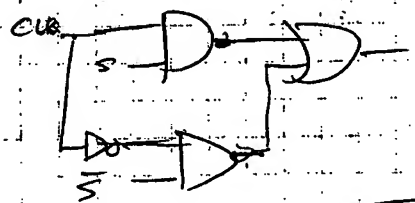


[redacted]

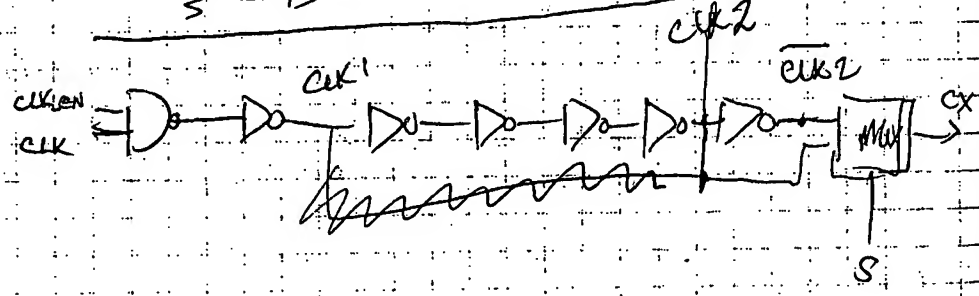
(2) refclk inversion - selectable



$$CX = CLK\,S + \overline{CLK}\,\overline{S}$$



(?)



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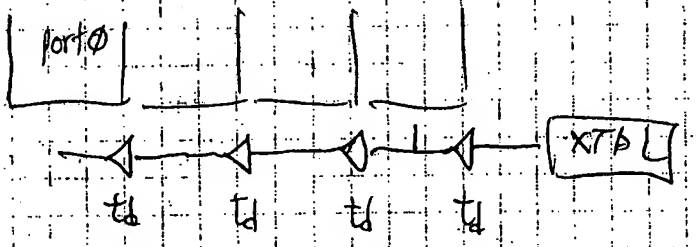
TXDAC phisel

ch0	ch1	ch2	ch3
0	180	0	180

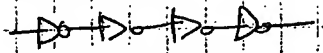
Reg 30_33:15:12 = 1010 (3210)

TBG init

4 ports

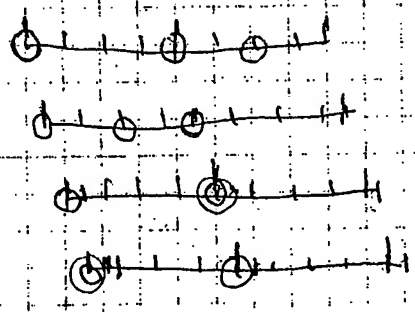


t_d = 4 inverts

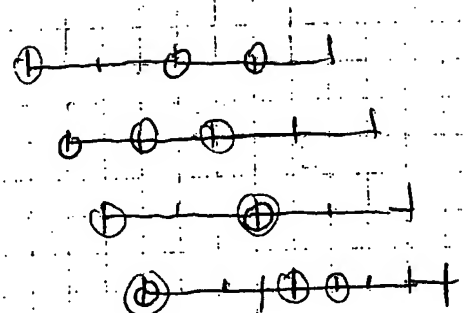


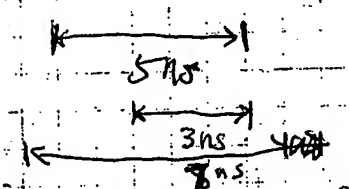
t_d = varies from 0.4ns → 1.0ns

t_d = 0.4ns



$t_d = 1\,ns$





best choice is 180°, 0°, 180°, 0° (3210)

9 ports

$t_d = 0.5ns$